



AVANTHI INSTITUTE OF ENGINEERING AND TECHNOLOGY

(Approved by A.I.C.T.E., New Delhi, & Permanently Affiliated to J.N.T.U-GV, Vizianagaram)

NAAC "B++" Accredited Institute

Cherukupally (Village), Near Tagarapavalasa Bridge, Vizianagaram (Dist) -531162.

www.aietta.ac.in, principal@aietta.ac.in

Department of Electronics and Communication Engineering

Program: M.Tech - VLSI-Design

Regulation: R16

Course Outcomes

No. of Courses: 23

| I-I Sem | Course: Digital System Design |
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| CO-1 | Understand the basic Physics and Modelling of MOSFETs. |
| CO-2 | Learn the basics of Fabrication and Layout of CMOS Integrated Circuits. |
| CO-3 | Study and analyze the performance of CMOS Inverter circuits on the basis of their operation and working. |
| CO-4 | Study the Static CMOS Logic Elements. |
| CO-5 | Study the Dynamic Logic Circuit Concepts and CMOS Dynamic Logic Families. |
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| I-I Sem | Course:VLSI Technology and Design |
| CO-1 | Understand the basic theory of MOS Transistors, basic steps of fabrication. Learn the basic theory of Crystal growth and preparation. |
| CO-2 | Understand the uses of formation and process of silicon dioxide growth, all important Tube furnaces. To learn different types oxidation such as Chemical vapor Deposition, and LPCVD of poly silicon. Oxidation, Kinetics of oxidation |
| CO-3 | Understand the series of processes that establishes the shapes, dimensions and placement of required physical components of IC on the wafer surface layer, understands different types lithography. |
| CO-4 | Learn formation of specific "Pockets" of conductive region and N-P in and on the wafer surface, understands the principles and practice of the two doping techniques, diffusion and ion implantation. |
| CO-5 | Understand the effect of contaminations on device processing, device performance. |
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| I-I Sem | Course: CMOS Analog IC Design |
| CO-1 | Apply knowledge of mathematics, science, and engineering to design and analysis of analog integrated circuits. |
| CO-2 | Identify, formulates, and solves engineering problems in the area of analog integrated circuits. |
| CO-3 | Use the techniques, skills, and modern programming tools such as Mentor Graphics, necessary for engineering practice. |
| CO-4 | Participate and function within multi-disciplinary teams. |
| CO-5 | Design a various stages of Operational amplifiers using CMOS devices. |
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| I-I Sem | Course: CMOS Digital IC Design |



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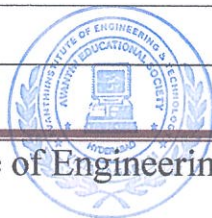
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| CO-1 | Identify the various IC fabrication methods. |
| CO-2 | Express the Layout of simple MOS circuit using Lambda based design rules. |
| CO-3 | Apply the Lambda based design rules for subsystem design. |
| CO-4 | Differentiate various FPGA architectures. |
| CO-5 | Design an application using Verilog HDL. |
| I-I Sem Course: Digital Design using HDL (Elective-I) | |
| CO-1 | Understand the language constructs and programming fundamentals of Verilog HDL. |
| CO-2 | Choose the suitable abstraction level for a particular digital design. |
| CO-3 | Construct Combinational and sequential circuits in different modelling styles using Verilog HDL. |
| CO-4 | Analyse and Verify the functionality of digital circuits/systems using test benches. |
| CO-5 | Understand the difference between simulation and synthesis environments. |
| I-I Sem Course: Advanced Operating Systems (Elective –I) | |
| CO-1 | List the principles of distributed systems and describe the problems and challenges associated with these principles. |
| CO-2 | Understand Distributed Computing techniques, Synchronous and Processes. Apply Distributed web-based system. |
| CO-3 | Apply Shared Data access and Files concepts. |
| CO-4 | Design a distributed system that fulfills requirements with regards to key distributed systems properties. |
| CO-5 | Understand Distributed File Systems and Distributed Shared Memory. |
| I-I Sem Course: Soft Computing Techniques (Elective –I) | |
| CO-1 | Develop intelligent systems leveraging the paradigm of soft computing techniques. |
| CO-2 | Implement, evaluate and compare solutions by various soft computing approaches for finding the optimal solutions. |
| CO-3 | Recognize the feasibility of applying a soft computing methodology for a particular problem |
| CO-4 | Design the methodology to solve optimization problems using fuzzy logic, genetic algorithms and neural networks. |
| CO-5 | Design hybrid system to revise the principles of soft computing in various applications |





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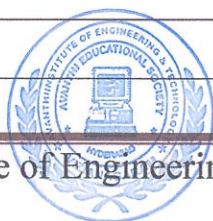
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| I-I Sem | Course: Cyber Security (Elective –I) |
| CO-1 | Analyze and evaluate the cyber security needs of an organization. |
| CO-2 | Determine and analyze software vulnerabilities and security solutions to reduce the risk of exploitation. |
| CO-3 | Measure the performance and troubleshoot cyber security systems. |
| CO-4 | Implement cyber security solutions and use of cyber security, information assurance, and cyber/computer forensics software/tools. |
| CO-5 | Comprehend and execute risk management processes, risk treatment methods, and key risk and performance indicators. |
| I-I Sem | Course: CPLD and FPGA Architectures and Applications (Elective –II) |
| CO-1 | Gain the knowledge about PLDs, FPGA Design & architectures. |
| CO-2 | Understand different types of arrays. |
| CO-3 | Learn FSM and different FSM techniques like petrinets, and different case studies. |
| CO-4 | Study different case studies using one hot design methods. |
| CO-5 | Familiarize various complex programmable Logic devices of different families. |
| I-I Sem | Course: Advanced Computer Architecture (Elective –II) |
| CO-1 | Demonstrate concepts of parallelism in hardware/software. |
| CO-2 | Discuss memory organization and mapping techniques. |
| CO-3 | Describe architectural features of advanced processors. |
| CO-4 | Interpret performance of different pipelined processors. |
| CO-5 | Explain data flow in arithmetic algorithms. |
| I-I Sem | Course: Hardware Software Co-Design (Elective –II) |
| CO-1 | Apply knowledge of mathematics, science, and engineering to computer engineering . |
| CO-2 | Design and conduct computer engineering experiments, as well as to analyze and interpret data. |
| CO-3 | Design a system, component, or process to meet desired needs. |
| CO-4 | Identify, formulate, and solve electrical computer problems |
| CO-5 | Use the techniques, skills, and modern engineering tools necessary for computer engineering practice. |





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| I-I Sem | Course: Front end VLSI Design Lab |
| CO-1 | Understand the physical design process of Digital Integrated Circuits. |
| CO-2 | Describe procedure for designing of programmable circuits. |
| CO-3 | Demonstrate the ability to use various EDA tools for digital system design. |
| I-II Sem | Course: VCMOS Mixed Signal Circuit Design |
| CO-1 | Present scenario presence mixed signal circuits because commercial and industrial application based on same. |
| CO-2 | Learn communication systems and digital processing mixed circuit being used. |
| CO-3 | Use RF IC design mixed signal circuit in highly appreciable. |
| CO-4 | Understand VLSI, based on Mixed signal circuits. |
| CO-5 | Apply Software for CAD in VLSI based on mixed signal circuits deign. |
| I-II Sem | Course: Embedded System Design |
| CO-1 | Acquire a basic knowledge about fundamentals of microcontrollers. |
| CO-2 | Acquire a basic knowledge about programming and system control to perform a specific task. |
| CO-3 | Acquire knowledge about devices and buses used in embedded networking |
| CO-4 | Develop programming skills in embedded systems for various applications. |
| CO-5 | Acquire knowledge about basic concepts of circuit emulators. |
| I-II Sem | Course: Low Power VLSI Design |
| CO-1 | Introduce low power VLSI design-Need for low power-CMOS leakage currentstatic. |
| CO-2 | Deal with Pre-computation logic |
| CO-3 | Discuss Power reduction in clock networks- CMOS floating node- low power busdelay balancing- SRAM. |
| CO-4 | Understand Algorithm and architectural level methodologies- Introduction, design flow |
| CO-5 | Discuss different type deign style. |
| I-II Sem | Course: Design For Testability |
| CO-1 | Give knowledge about testing process at IC level with their functions and relations. |
| CO-2 | Introduce the major concepts of all test techniques such as redundancy, fault coverage, sensitization and backtracking. |



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| CO-3 | Discuss test generation for combinational and sequential circuits both it examines in detail various techniques available for fault detection. |
| CO-4 | Deal with test generation and response evaluation techniques used in built-in-self-test (BIST) Schemes for VLSI chips some popular BIST architectures are examined. |
| CO-5 | Discuss the fundamental of fault detection and also introduces the concept of controllability, observably and fault equivalency. |
| I-II Sem Course: CAD for VLSI(Elective – III) | |
| CO-1 | Demonstrate knowledge and understanding of fundamental concepts, Graph Theory. |
| CO-2 | Demonstrate knowledge of computational and optimization algorithms and tools. |
| CO-3 | To solve CAD related problems. |
| CO-4 | Establish capability for CAD tool development and enhancement. |
| CO-5 | Get the Overview of Physical Design of VLSI ICs . |
| I-II Sem Course: DSP Processors & Architectures(Elective –III) | |
| CO-1 | To distinguish between the architectural features of general purpose processors and DSP processors. |
| CO-2 | Understand the architectures of TMS 320C54XX and ADSP2100 DSP devices. |
| CO-3 | Write assembly language programs using instruction set of TMS320C54XX. |
| CO-4 | Learn Interface of various devices to DSP Processors. |
| CO-5 | Develop the programming knowledge using Instruction set of DSP Processors. |
| I-II Sem Course: VLSI Signal Processing(Elective-III) | |
| CO-1 | To learn performance optimization techniques in VLSI signal processing. |
| CO-2 | Transformations for high speed and power reduction using pipelining, retiming, parallel processing techniques, supply voltage reduction as well as for strength or capacitance reduction. |
| CO-3 | Area reduction using folding techniques, Strategies for arithmetic implementation. |
| CO-4 | Synchronous, wave, and asynchronous pipelining. |
| CO-5 | Illustrate digital signals, systems and their significance. |
| I-II Sem Course: System on Chip Design(Elective – IV) | |
| CO-1 | Understand SoC Design Methodology |
| CO-2 | Understand the design of different embedded memories |



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| CO-3 | Validation and Testing Concepts can be understood. |
| CO-4 | Investigate new techniques for future system |
| CO-5 | Understand the concepts of System on Chip Design Validation |
| I-II Sem Course: Optimization Techniques in VLSI Design(Elective – IV) | |
| CO-1 | Learn the basics of MOS and CMOS technologies. |
| CO-2 | Design combinational logic circuits using MOS and CMOS technologies and develop stick and layout diagrams with design rules. |
| CO-3 | Calculate equivalent resistances and capacitances of circuits and estimate power consumption and delay. |
| CO-4 | Use Switch logic or Gate logic in their design projects. |
| CO-5 | Design the Combinational and Sequential circuits by using VHDL Language. |
| I-II Sem Course: Semiconductor Memory Design and Testing(Elective – IV) | |
| CO-1 | Analyse the different RAM and ROM architecture and interconnects. |
| CO-2 | Analyse about design and characterization technique. |
| CO-3 | Analyse different memory testing and design for testability. |
| CO-4 | Identify new developments in semiconductor memory design. |
| CO-5 | Comprehend the low power design techniques and methodologies. |
| I-II Sem Course: Back end VLSI Design Lab | |
| CO-1 | Design CMOS logic circuits. |
| CO-2 | Simulate circuits within a CAD tool and compare to design specifications. |
| CO-3 | Analyze the results of logic and timing simulations and to use these simulation results to debug digital systems. |




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