3.3.4 Number of research papers per teacher in the Journals notified on UGC website during the last five years (8)							
S. NO	**Title of paper**	**Name of the author/s**	**Department of the teacher**	**Name of journal**	**Year of publication**	**ISBN/ISSN number**	**URL CODE**
1	Implementation of Area And Power Optimisation For AES Encryption And Decryption Module On FPGA	B.NAVEEN	ECE	(IJITR) INTERNATIONAL JOURNAL OF INNOVATIVE TECHNOLOGY AND RESEARCH	2016-17	2320-5547	http://www.ijitr.com/index.php/ojs/article/view/1675
2	Estimating The Occupancy In Smart Buildings With The Help Of IOT-Based Techniques	P.SATEESH KUIMAR	ECE	*IJMETMR*	2016-17	2348-4845	http://www.ijmetmr.com/olnovember2016/VenkataraoDadi-PSateeshKumar-VSuresh-MKesabChandrasen-52.pdf
3	Estimating The Occupancy In Smart Buildings With The Help Of IOT-Based Techniques	V.SUESH	ECE	*IJMETMR*	2016-17	2348-4845	http://www.ijmetmr.com/olnovember2016/VenkataraoDadi-PSateeshKumar-VSuresh-MKesabChandrasen-52.pdf
4	Estimating The Occupancy In Smart Buildings With The Help Of IOT-Based Techniques	M.K.CHANDRASEN	ECE	*IJMETMR*	2016-17	2348-4845	http://www.ijmetmr.com/olnovember2016/VenkataraoDadi-PSateeshKumar-VSuresh-MKesabChandrasen-52.pdf
5	Design Of An POWER And Time Efficient Router By Using FSM	P.SATEESH KUIMAR	ECE	(IJITR) INTERNATIONAL JOURNAL OF INNOVATIVE TECHNOLOGY AND RESEARCH	2016-17	2320-5547	http://www.ijitr.com/index.php/ojs/article/view/1247
6	Estimating The Occupancy In Smart Buildings With The Help Of IOT-Based Techniques	M.K.CHANDRASEN	ECE	*IJMETMR*	2016-17	2348-4845	http://www.ijmetmr.com/olnovember2016/VenkataraoDadi-PSateeshKumar-VSuresh-MKesabChandrasen-52.pdf
7	Design Of An POWER And Time Efficient Router By Using FSM	P.SATEESH KUIMAR	ECE	(IJITR) INTERNATIONAL JOURNAL OF INNOVATIVE TECHNOLOGY AND RESEARCH	2016-17	2320-5547	http://www.ijitr.com/index.php/ojs/article/view/1247
8	Modeling and dynamic control of DFIG with integrated BESS through LVRT behavior	G.Venkata Ratnam	EEE	IOSR	2016-17	2348-4	http://www.iosrjournals.org/iosr-jeee/Papers/Vol11%20Issue%206/Version-1/C1106012128.pdf
9	Modeling and dynamic control of DFIG with integrated BESS through LVRT behavior	Jayaraju.M			2016-17	2348-4	http://www.iosrjournals.org/iosr-jeee/Papers/Vol11%20Issue%206/Version-1/C1106012128.pdf

10	Fuzzy based current controlled grid connected seven level inverter with RES	G.Giridhar Reddy	EEE	IOSR	2016-17	2319-8354	http://ijsetr.com/uploads/241365IJSETR8811-135.pdf
11	Simulation comparision of PWM control strategies for three phase seven level inverter	G.Giridhar Reddy	EEE	IJARSE	2016-17	2319-8354	http://ijsetr.com/uploads/345261IJSETR8846-189.pdf
12	Hardware Implementation of3- Phase Three Level Diode Clamped MLI Using SVPWM Technique	D.Dhan Prasad	EEE	IJARSE	2016-17	2320-9569	http://www.ijetee.org/Docs/Volume%2012/Issue%209/1.pdf
13	Design and analysis of grid connected photovoltaic system for step-up resonant convertor	A.Arjun Rao	EEE	IJETEE	2016-17	2348-795X	https://edupediapublications.org/journals/index.php/IJR/article/download/6492/6277
14	Simulation of Photovoltaic Cell with Back up Battery Storage System using Matlab	D.Dhan Prasad	EEE	IJR	2016-17	2348-4845	http://www.ijmetmr.com/olaugust2017/PPriyanka-DDhanaPrasad-17.pdf
15	Modeling and dynamic control of DFIG with integrated BESS through LVRT behavior	Shaik Shaheem	EEE	IJ&MET	2016-17	2348-4	http://www.iosrjournals.org/iosr-jeee/Papers/Vol11%20Issue%206/Version-1/C1106012128.pdf
16	*FPGA Implementation Of Peak Detector, 64 Bit BCD Counter And Reset Automatic Block For Pd Detection System Using VHDL Simulation*	P.SATEESH KUIMAR	ECE	*IJMETMR*	2015-16	2348-4845	http://www.ijmetmr.com/oljanuary2016/PSateeshKumar-MKesabChandrasen-VSuresh-VRaviTejesvi-86.pdf
17	*FPGA Implementation Of Peak Detector, 64 Bit BCD Counter And Reset Automatic Block For Pd Detection System Using VHDL Simulation*	P.SATEESH KUIMAR	ECE	*IJMETMR*	2015-16	2348-4845	http://www.ijmetmr.com/oljanuary2016/PSateeshKumar-MKesabChandrasen-VSuresh-VRaviTejesvi-86.pdf
18	*Design Of Automatic Number Plate Recognition System Using OCR For Vehicle Identification*	M.K.CHANDRASEN	ECE	*IJMETMR*	2015-16	2348-4845	http://www.ijmetmr.com/oljanuary2016/MKesabChandrasen-PSateeshKumar-KSGuruMurthy-VRaviTejesvi-80.pdf
19	*FPGA Implementation Of Peak Detector, 64 Bit BCD Counter And Reset Automatic Block For Pd Detection System Using VHDL Simulation*	M.K.CHANDRASEN	ECE	*IJMETMR*	2015-16	2348-4845	http://www.ijmetmr.com/oljanuary2016/PSateeshKumar-MKesabChandrasen-VSuresh-VRaviTejesvi-86.pdf
20	*LPC and Wavelet Techniques for Speech Compression*	V.RAVITEJESVI	ECE	*IJMETMR*	2015-16	2348-4845	http://www.ijmetmr.com/oljanuary2016/BRaviKiran-DLakshmiNarayana-BNaveen-VRaviTejesvi-87.pdf
21	*A Digital Systems Design of Simple Traffic Light Controller*	M.K.CHANDRASEN	ECE	*IJMETMR*	2015-16	2348-4845	http://www.ijmetmr.com/oljanuary2016/MKesabChandrasen-PSateeshKumar-VSuresh-DLakshmiNarayana-79.pdf

22	*A Digital Systems Design of Simple Traffic Light Controller*	V.SURESH	ECE	*IJMETMR*	2015-16	2348-4845	http://www.ijmetmr.com/oljanuary2016/MKesabChandrasen-PSateeshKumar-VSuresh-DLakshmiNarayana-79.pdf
23	*FPGA Implementation Of Peak Detector, 64 Bit BCD Counter And Reset Automatic Block For Pd Detection System Using VHDL Simulation*	V.SURESH	ECE	*IJMETMR*	2015-16	2348-4845	http://www.ijmetmr.com/oljanuary2016/PSateeshKumar-MKesabChandrasen-VSuresh-VRaviTejesvi-86.pdf
24	High Capacity Image Steganography in Wavelet Domain	V.SURESH	ECE	*IJMETMR*	2015-16	2348-4845	http://www.ijmetmr.com/oljanuary2016/DLakshmiNarayana-KSGuruMurthy-BRaviKiran-VSuresh-81.pdf
25	LPC and Wavelet Techniques for Speech Compression	B.NAVEEN	ECE	*IJMETMR*	2015-16	2348-4845	http://www.ijmetmr.com/oljanuary2016/BRaviKiran-DLakshmiNarayana-BNaveen-VRaviTejesvi-87.pdf
26	A Digital CMOS Parallel Counter Architecture	A.LEELAVATHI	ECE	IJMTER	2015-16	2349-9745	https://www.ijmter.com/papers/volume-3/issue-2/a-digital-cmos-parallel-counter-architecture.pdf
27	*FPGA Implementation Of Peak Detector, 64 Bit BCD Counter And Reset Automatic Block For Pd Detection System Using VHDL Simulation*	P.SATEESH KUMAR	ECE	*IJMETMR*	2015-16	2348-4845	http://www.ijmetmr.com/oljanuary2016/PSateeshKumar-MKesabChandrasen-VSuresh-VRaviTejesvi-86.pdf
28	*Design Of Automatic Number Plate Recognition System Using OCR For Vehicle Identification*	P.SATEESH KUIMAR	ECE	*IJMETMR*	2015-16	2348-4845	http://www.ijmetmr.com/oljanuary2016/MKesabChandrasen-PSateeshKumar-KSGuruMurthy-VRaviTejesvi-80.pdf
29	*A Digital Systems Design of Simple Traffic Light Controller*	P.SATEESH KUIMAR	ECE	(IJITR) INTERNATIONAL JOURNAL OF INNOVATIVE TECHNOLOGY AND RESEARCH	2015-16	2348-4845	http://www.ijmetmr.com/oljanuary2016/MKesabChandrasen-PSateeshKumar-VSuresh-DLakshmiNarayana-79.pdf
30	High speed electric drive with multilevel inverter for exhaust gas energy recovery applications	G.Giridhar Reddy K.Tarakeshwar Rao	EEE	IJSETR	2015-16	2319-8885	http://ijsetr.com/uploads/645132IJSETR7622-1710.pdf
31	Simulation of bridgeless buck-boost convertor fed BLDC motor with fuzzy logic controller	G.Giridhar Reddy V.Siva Ramakrishna	EEE	IJSETR	2015-16	2319-8885	http://ijsetr.com/uploads/325164IJSETR7623-1711.pdf
32	Minimising of fault curent uisng SFCL with PV based distributed generation scheme	G.Prasanth S.Manasa	EEE	IJMETMR	2015-16	2348-4845	http://www.ijmetmr.com/olnovember2015/SManasa-GPrasanth-83.pdf
33	Fuzzy based DC voltage controller for high power STATCOM with asymmetric Twin convertors	G.V.Phanindra P.Sagar	EEE	IJSETR	2015-16	2278-7798	http://ijsetr.org/wp-content/uploads/2015/11/IJSETR-VOL-4-ISSUE-11-3856-3863.pdf
34	Hystersis voltage controller technique based on dynamic voltage restorer for compensation of voltage sag and Swell conditions	G.V.Phanindra Y.Priyanka	EEE	IJSETR	2015-16	2319-8885	http://ijsetr.com/uploads/512364IJSETR7685-1790.pdf

35	Performance of PhotovoltaicAssisted Five Level Diode Clamped Inverter fed Induction Motor	D.Dhan Prasad	EEE	IJMTST	2015-16	2455-3778	http://www.ijmtst.com/documents/40.IJMTST020509.pdf
36	Performance of Photovoltaic Assisted Five Level Diode Clamped Inverter fed Induction Motor	A.Krishna Veni	EEE	IJMTST	2015-16	2455-3778	http://www.ijmtst.com/documents/40.IJMTST020509.pdf
37	Analysis of closed loop control of high voltage gain DC-DC bosst convertor using voltage multiplier devices for variable voltage applications	A.Arjun Rao, B.Bangaru Naidu	EEE	IJSETR	2015-16	2319-8885	http://ijsetr.com/uploads/124356IJSETR7618-1706.pdf
38	Fuzzy control backpropogation algorithm based Dstatcom for power Quality	A.Arjun Rao,A.S.L.K.Gopalamma	EEE	IJATIR	2015-16	2348-237U	http://www.ijatir.org/uploads/162543IJATIR7674-533.pdf
39	An optimized fully dynamic latched comparator for high speed flash and pipeline data conversion application	V.RAVITEJESVI	ECE	*International Journal of Engineering Research & Technology (IJERT)*	2014-15	2278-0181	https://www.ijert.org/browse/volume-3-2014/november-2014-edition
40	*High Performane UDVS8-1 SRAM Design With Write And Read Assistant Schemes*	P.SATEESH KUMAR	ECE	*International Journal Of Scientific Research And Education*	2014-15	2321-7545	http://ijsae.in/ijsaeems/index.php/ijsae/article/view/599
41	Design and model of sensorless vector controlled induction motor using model reference adaptive systems	P.Janaki	EEE	IJARSE	2014-15	2319-8354	https://www.ijarse.com/images/fullpdf/1406734405_31_DESIGN_AND_MODELLING_OF_SENSORLESS_VECTOR_CONTROLLED_INDUCTION_MOTOR_USING_MODEL_REFERENCE_ADAPTIVE_SYSTEMS.pdf
42	Super capacitor energy storage of DFIG wind turbines with fuzzy controller	A.Arjun Rao	EEE	IJERD	2014-15	2278-800X	http://www.ijerd.com/paper/vol10-issue12/Version_2/H10125266.pdf
43	Optimisation and simulation of electric ship with low voltage AC-DC Hybrid power system	A.Arjun Rao	EEE	IJSR	2014-15	2319-7064	https://www.ijsr.net/archive/v3i12/U1VCMTQ5NTk=.pdf
44	Implementation Of Fpga Based 32-Bit Cisc Cpu Design	M.K.CHANDRASEN	ECE	*International Journal Of ADVANCE RESEACH in computer science and management studies*	2013-14	2278-1021	https://ijarcce.com/wp-content/uploads/2012/03/IJARCCE8E-a-saraswathi-Implementation.pdf

45	Verilog Implementation Of 32 Point FFT Using Radix-2	V.RAVITEJESVI	ECE	*IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)*	2013-14	2347 - 1778	https://pdfs.semanticscholar.org/f83c/394ddc4780d6fa9b47411440689cd213c64c.pdf
46	Verilog Implementation Of 32 Point FFT Using Radix-2	G.ANANTH RAO	ECE	*IOSR Journal of Electronics and Communication Engineering (IOSR-JECE)*	2013-14	2347 - 1778	https://pdfs.semanticscholar.org/f83c/394ddc4780d6fa9b47411440689cd213c64c.pdf
47	Implementation Of Novel Difference set code for major fault Detection	A.MADHUSUDHANA RAO	ECE	International Journal Of Advanced Research In Computer And Communication Engineering	2013-14	2319-5940	https://ijarcce.com/wp-content/uploads/2012/03/IJARCCE5G-S-NAV_IMPLEMENTATION_OF.pdf
48	Effective Implementation of SHA-1 Algorithm using FPGA	K.SYAMALA	ECE	International Journal Of Advanced Research In Computer And Communication Engineering	2013-14	2319-5940	https://ijarcce.com/wp-content/uploads/2012/03/IJARCCE6J__s_Nav_sunil_45_effective.pdf
49	A novel control strategy for grid connected VSC with LCL filters	A.Arjun Rao	EEE	IJEDR	2013-2014	2321-9939	https://www.ijedr.org/papers/IJEDR1404023.pdf
50	Integration of DG hybrid microgrid with power balancing control using CHB multi level inverter under various loads	A.Arjun Rao	EEE	IJE	2013-2014	2321-9939	https://www.ijedr.org/papers/IJEDR1404014.pdf
51	A novel control strategy for power quality improvement using ANN technique for microgrid	A.Arjun Rao	EEE	IJERD	2013-2014	2278-067X	http://www.ijerd.com/paper/vol10-issue11/Version_4/A10110113.pdf